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Amendment dated October 17, 2005

REMARKS/ARGUMENTS

Claim 1 stands rejected for being obvious over the teachings of US Patent 6,205,155 (hereinafter "Parrella") in view of US Patent 6,622,182 (hereinafter "Miller"). In explaining the rejection of Claim 1, the Examiner relied on Parrella as the primary reference, for disclosing "an arbitration apparatus with backpressure capability." The Examiner stated that Parrella did not disclose incrementing and decrementing of counters, and then cited Miller. Then the Examiner referred to Miller's credit counter 315 for a teaching that the traffic source knows how much information can be sent to the destination without overflowing the destination's buffer.

Claim 1 as amended above is believed to distinguish over the combined teachings of Parella and Miller. Reconsideration is respectfully requested.

Claim 1 now states that multiple traffic sources receive packet grants from an arbiter, to be used to release packets on multiple buses to an asynchronous cross-point switch, for transfer therethrough. Specifically, Claim 1 as now amended states that the arbiter issues packet grants to multiple traffic sources. It is in response to the packet grants that the multiple traffic sources (which maintain VOQs) release packets destined to particular output ports of the claimed cross-point switch, on corresponding multiple buses.

Parrella fails to disclose or suggest the architecture described in the previous paragraph. Specifically, Parrella's element 10 shown in his Figure 1 has been analogized to Claim 1's arbiter, at the bottom of page 2 of the Office Action, citing to Parrella's column 3 lines 28-40 and 60-65; column 4, lines 13-17. However, Parrella describes element 10 as a bus master. Applicants submit that Parrella's bus master 10 is not an arbiter, as this term is used in Claim 1. For example, Parrella's bus master 10 merely allows a single traffic source to access his single bus (to multiple outputs). In contrast, Claim 1's switch is coupled to multiple buses that are accessed by multiple traffic sources, as per packet grants by the arbiter.

Moreover, Miller fails to overcome the just-described defect in Parrella's teachings. Specifically, Miller's FIG. 2 was cited in the middle of page 3 of the Office Action. However, in this figure, Miller merely discloses a computer controlled input/output system which appears to have a processor 20 coupled to memory controller 205 that in turn is coupled to a cross-bar switch 220, and switch 220 in turn is coupled to an input/output unit

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230. Miller's FIG. 2 fails to disclose or suggest an asynchronous cross-point switch having multiple buses coupled to multiple traffic sources. Even accepting the Examiner's characterization of processor 201 as a traffic source, and memory controller 205 as the arbiter as stated in line 5-6 on page 4 of the Office Action, Miller at most teaches that his traffic source 201 is coupled to his arbiter 205, and not to his switch 220 (to which input/output unit 230 is coupled). So, even under the Examiner's interpretation, Miller's FIG. 2 fails to disclose or suggest a multi-bus star configuration with a switch in the center, e.g. nothing to suggest buses 280 and 281 are coupled to switch 220.

In explaining the application of Miller's teachings, in the bottom half of page 4 of the Office Action, the Examiner cited to Miller's Figures 4 and 5, and cited to Miller's column 7 lines 25-27 and 35-40. In the cited text and drawings, Miller merely appears to teach a flow control mechanism for transfer of data from a single traffic source. In such data transfer, the source (processor 201) apparently knows that it is the only device writing into the destination (buffer 230a). Therefore, processor 201 operates without concern that another traffic source may write to and fill up buffer 230a. Hence, there is no need for explicit grants, prior to transfer of data by processor 201.

Moreover, Miller doesn't disclose or suggest that an explicit grant mechanism should be used. Applicant respectfully traverses the Examiner's unsupported statement "using the terminology of the applicant a grant must first occur in order for a packet to initially leave the source buffer and finally reach the destination input/output buffer" (see bottom paragraph on page 4 of the Office Action). The Examiner has not provided any prior art basis for treating Miller's packet leaving FIFO buffer 201a as being "equivalent" to applicant's packet grant.

Applicant also respectfully traverses the Examiner's use of two of applicant's own claim limitations to support the Examiner's interpretation of prior art (see the bottom of page 4 and the top of page 5 of the Office Action). The Examiner's interpretation must be supported by prior art, not by applicant's own claim !!!

Specifically, the Examiner's position that the claimed issuance of a packet grant is interchangeable with Miller's packet leaving buffer 201a, is incorrect at least because it assumes a loss-less and a delay-less system (e.g. what happens if a packet grant were to be lost and a corresponding packet doesn't leave; also even if the proposed system were

SILICON VALLEY
PATENT GROUP LLP2350 Mission College Blvd.
Suite 300
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

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loss-less, how to account for the latency between issuance of a packet grant and transmission of the packet from buffer 201a). Similarly, the Examiner's position that a packet leaving buffer 201a is interchangeable with storing the packet in a destination buffer is incorrect.

The Examiner readily admits that Miller's "traffic source does not need a special grant signal from the arbiter ..." (see last paragraph on page 5 of the Office Action). Hence, the Examiner has himself stated that the packet grants as recited in Claim 1 are nowhere disclosed or suggested by Miller. Therefore, there is no indication by Miller to keep a count of packet grants. At most Miller teaches counting of packets (when a packet leaves buffer 201a), but not counting of packet grants. Moreover, Parrella fails to overcome this defect in Miller's teachings. Hence, the combined teachings of Parrella and Miller fail to disclose or suggest an explicit limitation in Claim 1, namely incrementing of grant counters.

Applicant also respectfully traverses the Examiner's suggestion to combine the teachings of Parrella and Miller for the motivation of "efficient utilization of the buffer space at the destination by preventing buffer overflow and limiting unnecessary interrupts to the flow control mechanism." Specifically, Parrella teaches use of packet counters, which are adequate to provide an efficient utilization of destination buffer space. The Examiner has not shown why Parrella's counters are insufficient, and why they should be replaced with Miller's counters.

Even if the Examiner's combination is appropriate, the Office Action fails to state how the teachings of Miller are to be extended from Parrella's single bus master 10, to a multi-bus architecture. In making such an extension, the following questions should be answered: (1) why extend to multiple buses? (2) will there be multiple bus masters, one for each of the multiple buses or will there be a single bus master for all buses? (3) if a single bus master, then does it stall traffic on all buses from all input ports or grant access to a specific input port that is associated with the output port in danger of overflowing? In answering such questions, the Examiner may not use Applicant's invention, and instead must cite to prior art.

Two answers to question (3) above teach away from the invention as recited in Claim 1. Specifically, Claim 1 requires instructing the arbiter to cease issuing grants for

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packets having an output port as destination once a corresponding grant counter for the output port has exceeded a predetermined threshold. Thus an arbiter operating in accordance with Claim 1's instruction, may grant access to any input port whose packet is not destined to an overflowing output port. Such packet-level arbitration of bus access by the arbiter is made possible by the VOQ architecture recited in Claim 1. In the absence of VOQ, it is unlikely for a prior art arbiter, of the type taught by Parrella and Miller, to arbitrate access to multiple buses.

In view of the above remarks, Applicant respectfully requests the Examiner to withdraw the prior art rejection of Claim 1, as well as the rejection of Claims 2-5 that depend from Claim 1. New Claims 12-19 are believed to be patentable over the cited prior art by Parrella and Miller for similar reasons.

In the above-identified Office Action, at the bottom of page 8, in paragraph 9, the Examiner cited to paragraphs 17, 19, 41 and Figures 5-7 of Assa for disclosing negating the instruction to the arbiter to cease issuing grants, based on a hysteresis setting, thereby to start issuing grants again after the instructing. In paragraph 19 (cited by the Examiner), Assa states that "Whenever the buffer is filled up to the maximum level it enters a Blocking State, during which any incoming data cells are discarded. Whenever the buffer is emptied down to below its hysteresis level, it switches to an Absorbing State...The cycle of switching between the two states repeats as long as the incoming rate exceeds the outgoing rate ..." Therefore, at most Assa teaches use of hysteresis to discard data.

Assa fails to disclose or suggest use of hysteresis in situations that do not involve discarding of data. Specifically, Claim 2 requires negating the instruction to the arbiter to cease issuing grants, based at least on a hysteresis setting. On negation of the cease grants instruction, the arbiter may be expected to return to issuing grants again. While grants are being issued, data is transmitted, thereby to eliminate any need to discard the data. Use of hysteresis to change grant behavior of the arbiter is nowhere disclosed or suggested by Assa. Hence, Claim 2 is believed to be patentable over Assa's teaching. Claim 2 is further amended herewith to require discarding a packet if an input buffer in a traffic source has not been read when a time out occurs. Support for this amendment is found in, for example, page 10 at lines 20-26. The combination of limitations now recited

SILICON VALLEY
PATENT GROUP LLP1350 Mission College Blvd
Suite 360
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210

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in Claim 2 (which includes Claim 1), is nowhere found in Assa alone or in combination with Miller and Parrella.

Applicant also respectfully traverses the Examiner's suggestion to combine the teachings of Assa with the teachings of Parrella and Miller for the Examiner-stated motivation of "being able to store in the buffer a complete frame and consequently guaranteeing a high throughput of complete packets." Specifically, there is no indication in Parrella that his buffers are too small to hold a complete frame (FIG. 2). In fact, Parrella states (at top of column 7) that even when a buffer is limited to small size, it can hold 10 milliseconds of buffering. As will be apparent to the skilled artisan, a frame is transmitted in considerably less than 10 milliseconds. Therefore, there is nothing in Parrella to support the Examiner's suggestion that Parrella's teachings must be modified, so as to store in the buffer a complete frame. Moreover, Miller states that his buffers can have a variety of sizes, such as 1K, 2K, 4K, 8K etc, each of which is sufficiently large to hold a frame. Therefore, there is nothing in Miller to support the Examiner's suggestion that Parrella's and Miller's teachings must be modified, so as to store in the buffer a complete frame. Hence, the Examiner has not shown a sufficient motivation to look to the teachings of Assa.

In the above-identified Office Action, at the top of page 10, in paragraph 11, the Examiner cited to Figures 1, 4, and 5 as well as column 7 lines 1-17 and column 8 lines 59-67 of Barkey for disclosing a method of periodically auditing the counter to avoid upward drift due to loss of packets. The Examiner stated that the motivation was "to ascertain whether credit loss or credit gain has occurred from a specified number of credits and to be able to automatically correct an ascertained credit loss or credit gain without resetting the system."

Applicant respectfully traverses the Examiner's suggestion to combine the teachings of Barkey with the teachings of Parrella and Miller. Specifically, as the Examiner acknowledged at pages 4 and 5 of the Office Action, Miller already discloses a credit mechanism. Miller further teaches that a correction can be made without resetting the system, by sending a signal to reset a timer unit and stop counting (see Miller's column 7, lines 56-62). Therefore, a skilled artisan would be motivated to simply use the mechanism already provided by Miller. Miller further states that it is wasteful to invoke a time consuming and process intensive interrupt service routine, thereby to teach away from

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implementing additional functionality, such as the audit mechanism proposed by the Examiner.

Moreover, even assuming the Examiner is correct in combining the teachings of Barkey with the teachings of Parrella and Miller, Applicant respectfully submits that the combined teachings fail to disclose or suggest an audit mechanism in the combination recited in Claim 4. Specifically, Barkey's step 50 in FIG. 2 has an initial decision point, namely is there any "data to send." Barkey at most teaches an audit mechanism for checking first (in step 50), before sending data (in step 54). Barkey fails to disclose or suggest an audit mechanism for an arbiter that issues packet grants based on VOQ images in the arbiter.

Accordingly, Applicant respectfully requests allowance of all pending claims. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 982-8203.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office to the fax number 571-273-8300 on October 17, 2005.

S. Omkar
Attorney for Applicant(s)

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Date of Signature

Respectfully submitted,

S. Omkar

Omkar K. Suryadevara
Attorney for Applicant(s)
Reg. No. 36,320

SILICON VALLEY
PATENT GROUP LLP

2350 Mission College Blvd
Suite 360
Santa Clara, CA 95054
(408) 982-8200
FAX (408) 982-8210